IN THE SPECIFICATION

Please amend Paragraph [0014] on Page 8, Line 22 to Page 9, Line 2 as follows.

[0014] ~~FIGURE 6~~ FIGURE 5 depicts an exemplary implementation for a block-based memory allocation, longest-prefix match, hashing IP lookup scheme according to one embodiment of the present invention; and

Please amend Paragraph [0017] on Page 10, Line 11 to Page 11, Line 2 as follows.

[0017] FIGURE 1 depicts a processing system utilizing a hash-based network search engine according to one embodiment of the present invention. Processing system 100 implements a portion of an Internet Protocol (IP) network router and includes a system processor/controller or network processing unit (NPU) 101 coupled to a network packet search engine (NPSE) 102, which in turn is coupled to external memories 103 and 104. Memory 103 is an overflow content addressable memory (CAM), while external memory [[103]] 104 holds next hop information. NPSE 102 receives addresses and/or commands from system controller 101 as well as prefixes for looking up the next hop address, and returns the next hop address to system controller 101. System controller 101 is coupled to a backplane 105 and through a network interface 106 to a network (not shown).